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| 10/049,792                                   | 02/14/2002  | Hironori Aoki        | 542-007-2           | 6079             |
| 4955                                         | 7590        | 02/15/2006           | EXAMINER            |                  |
| WARE FRESSOLA VAN DER SLUYS & ADOLPHSON, LLP |             |                      |                     | DUONG, THOI V    |
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**BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES**

**MAILED**

**FEB 15 2006**

**GROUP 2800**

Application Number: 10/049,792  
Filing Date: February 14, 2002  
Appellant(s): AOKI, HIRONORI

Milton Oliver (Reg. No. 28,333)  
For Appellant

**EXAMINER'S ANSWER**

This is in response to the appeal brief filed December 01, 2005 appealing from the  
Office action mailed June 16, 2004.

**(1) Real Party in Interest**

A statement identifying by name the real party in interest is contained in the brief.

**(2) Related Appeals and Interferences**

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

**(3) Status of Claims**

The statement of the status of claims contained in the brief is correct.

**(4) Status of Amendments After Final**

No amendment after final has been filed.

**(5) Summary of Claimed Subject Matter**

The summary of claimed subject matter contained in the brief is correct.

**(6) Grounds of Rejection to be Reviewed on Appeal**

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

**(7) Claims Appendix**

The copy of the appealed claims contained in the Appendix to the brief is correct.

**(8) Evidence Relied Upon**

|              |               |         |
|--------------|---------------|---------|
| US 6,078,366 | Dohjo et al.  | 6-2000  |
| JP 11-284195 | Sakata et al. | 10-1999 |

**(9) Grounds of Rejection**

The following ground(s) of rejection are applicable to the appealed claims:

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

**Claims 1-3, 5, 6, 8-12 and 15-18 are rejected under 35 U.S.C. 102(b) as being anticipated by Dohjo et al. (Dohjo, USPN 6,078,366).**

Re claim 1, as shown in Figs. 1, 3, 5 and 13, Dohjo discloses an array substrate 100 comprising:

a display area (TFT region) in which pixel electrodes 131 are formed,

a scanning line 111 formed of a low resistivity metal (col. 7, lines 16-27), said scanning line being arranged between the pixel electrodes 131,

a signal line 110 formed of a high melting point metal such as Mo, Ta or its alloy (col. 7, lines 28-37), said signal line crossing over the scanning line 111 interposing an insulating layer 115 therebetween,

a terminal 152 to which a scanning signal is applied, and

an extended scanning line 125a for connecting the scanning line 111 with the terminal 152, said extended scanning line being formed only of the same conductive film as for said signal line 110,

wherein, re claim 6, the extended scanning line 125a is electrically connected to the scanning line 111 through contact holes 153, 154 at the neighborhood of the display area and electrically connected to the terminal 152 for the scanning signal through contact holes 155, 156 at the neighborhood of the terminal (see Figs. 1 and 3);

wherein, re claim 15, the scanning line 111 and the extended scanning line 125a are electrically connected via a conductive film of the same layer 131 as that for the pixel electrode;

wherein, re claim 17, the extended scanning line 125a is formed in a grid like shape at a region (Base section in Fig. 3) in which the scanning line and the extended scanning line are overlapped within a connecting portion between the scanning line and the extended scanning line; and

where, re claim 12, aluminum or aluminum alloy is used for material of the scanning line (col. 7, lines 16-27);

Re claims 2 and 3, as shown in Figs. 28 and 31, the array substrate further comprises:

an auxiliary capacitance line 113 arranged in parallel to the scanning line 111 (Fig. 28 and col. 23, lines 54-55),

a collected auxiliary capacitance line (dotted line of storage capacitor-line connecting section 190 in Fig. 28) arranged in parallel to the signal line 110 and electrically connected to the auxiliary capacitance line 113,

a terminal to which a common signal is applied (at top left of Fig. 28), and

an extended auxiliary capacitance line 125 for connecting the collected auxiliary capacitance line with the terminal for the common signal (Fig. 31), said extended auxiliary capacitance line being formed only of the same conductive film as for said signal line (col. 23, lines 54-64),

wherein, re claims 5 and 8, the collected auxiliary capacitance line and the extended auxiliary capacitance line are electrically connected via a conductive film 193 of the same layer as that for the pixel electrode (Fig. 31);

wherein, re claim 9, the extended auxiliary capacitance line 125 is electrically connected to the collected auxiliary capacitance line at the neighborhood of the display area through a contact hole 192 and electrically connected to the terminal for the common signal through a contact hole 194 at the neighborhood of the terminal;

wherein, re claim 10, the auxiliary capacitance line 113, the collected auxiliary capacitance line and the scanning line 111 are formed from the conductive film of same layer (col. 23, lines 42-45);

wherein, re claim 11, the collected auxiliary capacitance line and the extended scanning line are crossing interposing an insulating layer 117 therebetween (Fig. 31); and

wherein, re claim 18, the extended auxiliary capacitance line 125 is formed in a grid like shape at a region 190 in which the collected auxiliary capacitance line and the extended auxiliary capacitance line are overlapped within a connecting portion between the collected auxiliary capacitance line and the extended auxiliary capacitance line (see Fig. 31).

Finally, re claim 16, Dohjo also discloses in another embodiment that the extended scanning line and the pixel electrodes are formed from the conductive film of same layer (col. 5, lines 27-45). Since the extended auxiliary capacitance line is formed at the same layer as the extended scanning line, the extended auxiliary capacitance line and the pixel electrodes are also formed from the conductive film of same layer.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

**Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dohjo et al. (Dohjo, USPN 6,078,366) in view of Sakata et al. (Sakata, JP 11-284195).**

Dohjo discloses an array substrate that is basically the same as that recited in claim 13 except that the material used for the scanning line is not nitridated aluminum or nitridated aluminum alloy. Sakata discloses a process in which impurity constituted of one of N, O, Si and C is added to an upper layer of a scanning line formed of pure aluminum or aluminum alloy to directly provide low contact resistance (paragraph 11).

Thus, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the array substrate of Dohjo with the teaching of Sakata by using partly or wholly nitridated aluminum or partly or wholly nitridated

aluminum alloy for the scanning lines so as to obtain a low contact resistance (see Abstract).

#### **(10) Response to Argument**

Applicant's arguments filed December 01, 2005 have been fully considered but they are not persuasive.

With respect to the section 102(b) rejection, Applicant argued that Dohjo teaches two alternatives, only one of which would be suitable for solving the "contact resistance" problem does not constitute an "anticipation by inherence" and that Dohjo does not mention "contact resistance". The Examiner disagrees with Applicant's remarks since Dohjo expressly discloses each and every limitation found in claims 1 and 3 of the invention. This conforms the requirement of Section 102 that "each and every limitation is found either expressly or inherently in a single prior art reference." In this case, Dohjo expressly anticipates the claimed invention where a signal line is formed of Mo-Ta alloy, which is a high melting point metal (col. 7, lines 35-37). However, since the structure of Dohjo is substantially identical to that of claims 1 and 3, claimed properties or functions (solving the contact resistance problem) are presumed to be inherent. Therefore, a *prima facie* of anticipation has been established (see MPEP 2112.01 and 2131). It is also noted that Applicant does not claim properties or functions in claims 1 and 3.

Applicant also argued that Dohjo accidentally included some high-melting-point alloys among his suggested electrode materials does not amount to a teaching that such materials are necessary or even preferable, and Dohjo nowhere distinguishes between wiring resistance and contact resistance. The Examiner disagrees since Dohjo

expressly anticipates the claimed invention, the Dohjo's reference is presumed operable (see MPEP 2121) and hence, the Dohjo's disclosure of some high-melting point alloys among his suggested materials is assumed valid. Nowhere in the Dohjo's reference indicates that the high-melting point is not "necessarily present" or not preferable in the Dohjo structure. Moreover, according to MPEP 2122, "in order to constitute anticipatory prior art, a reference must identically disclose the claimed compound, but no utility need be disclosed by the reference." Since Dohjo expressly discloses the claimed invention, there's no need for disclosing wiring resistance and contact resistance or suggesting that doping aluminum alloy would solve any contact resistance problem.

Finally, with respect to the section 103 rejection of claim 13, Applicant argued that there is no sufficient motivation to combines the two references since Dohjo does not appreciate the nature of the contact resistance problem and does not suggest combination with another disclosure to solve the problem. The Examiner again disagrees with Applicant's remarks since the Examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, Sakata discloses a process in which impurity constituted of one of N, O, Si and C is added to an upper layer of a scanning line formed of pure aluminum or aluminum alloy to directly provide low contact resistance (paragraph 11). Thus, it is obvious to one

having ordinary skill in the art at the time the invention was made to apply partly or whollynitridated aluminum alloy for scanning lines of Dohjo as taught by Sakata so as to obtain a low contact resistance in order to prevent delay of a signal for scanning line (see Abstract and paragraph 7), which is a reasonable expectation of success. Accordingly, this reasonable expectation has been founded in the Sakada's reference, not in the Applicant's disclosure.

For the above reasons, it is believed that the rejections should be sustained.

**(11) Related Proceeding(s) Appendix**

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

Respectfully submitted,



Thoi Duong

February 14, 2006

Note: An appeal conference was held on February 14, 2006 with the following conferees:

|                                                                                     |                               |                      |
|-------------------------------------------------------------------------------------|-------------------------------|----------------------|
|  | Drew Dunn, SPE AU 2872        | Date <u>2/14/06</u>  |
|  | Dave Porta, SPE AU 2884       | Date <u>02/14/06</u> |
|  | Thoi Duong, Examiner, AU 2871 | Date <u>02/14/06</u> |